AF/2188
IFW

Attorney's Docket No.: 42390.P6468C

Patent

In re the Application of: William R. Stafford
(inventor(s))

APPELLANT'S BRIEF UNDER 37 C.F.R. § 1.192

Application No.: 09/927,252

Filed: August 10, 2001

For: MULTIPLE USER INTERFACES FOR AN INTEGRATED FLASH DEVICE
(title)

Mail Stop Appeal Brief - Patents
Commissioner for Patents
PO Box 1450
Alexandria, Virginia 22313-1450

SIR: Transmitted herewith is an **Appellant's Brief Under 37 C.F.R. § 1.192** for the above application.

X **Appellant's Brief Under 37 C.F.R. § 1.192** in triplicate is enclosed.
X A check for $330.00 is attached for processing fees under 37 C.F.R. § 1.17 (f).
____ A check in the amount of $_____ is attached for presentation of additional claim(s).
____ Applicant(s) hereby Petition(s) for an Extension of Time of _____ month(s) pursuant to 37 C.F.R. § 1.136(a).
____ A check for _____ is attached for processing fees under 37 C.F.R. § 1.136 (a).
____ Please charge my Deposit Account No. 02-2666 the amount of $_____.
A duplicate copy of this sheet is enclosed.
X The Commissioner of Patents and Trademarks is hereby authorized to charge payment of the following fees associated with this communication or credit any overpayment to Deposit Account No. 02-2666 **(a duplicate copy of this sheet is enclosed)**:
  X Any additional filing fees required under 37 C.F.R. § 1.16 for presentation of extra claims.
  X Any extension or petition fees under 37 C.F.R. § 1.17.

BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP

Date: August 4, 2004

Daniel E. Ovanezian

Reg. No. 41,236

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA 90025(408)
720-8598

FIRST CLASS CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to Mail Stop Appeal Brief - Patents, Commissioner for Patents, PO Box 1450, Alexandria, Virginia 22313-1450.

on August 4, 2004 JUANITA BRISCOE
Date of Deposit Name of Person Mailing Correspondence

Signature 8/4/04
Date

FEE TRANSMITTAL FOR FY 2004

(FY 2004 Begins 10/01/2003)

TOTAL AMOUNT OF PAYMENT ($) $330.00

Complete if Known:

Application No. 09/927,252
Filing Date 8/10/01
First Named Inventor William R. Stafford
Examiner Name Song, Jasmine
Art Unit 2188
Attorney Docket No. 42390.P6468C

____ **Applicant claims small entity status. See 37 CFR 1.27.**

METHOD OF PAYMENT (check all that apply)

_____ **Check** _____ **Credit Card** _____ **Money Order** _____ **Other** _____ **None**

__X__ **Deposit Account**
Deposit Account Number : 02-2666
Deposit Account Name: _____

__X__ **The Director is Authorized to do the following with respect to the above-identified Deposit Account:**
____ **Charge fee(s) indicated below.**
__X__ **Credit any overpayments.**
__X__ **Charge any additional fees during the pendency of this application.**
__X__ **Any concurrent or future reply that requires a petition for extension of time should be treated as incorporating an appropriate petition for extension of time and all required fees should be charged.**
____ **Charge fee(s) indicated below except for the filing fee.**

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	770	2001	385	Utility application filing fee	_____
1002	340	2002	170	Design application filing fee	_____
1003	530	2003	265	Plant filing fee	_____
1004	770	2004	385	Reissue filing fee	_____
1005	160	2005	80	Provisional application filing fee	_____

SUBTOTAL (1) $_____

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

		Extra Claims		Fee from below		Fee Paid
Total Claims	_____	– 20** =	_____	X _____	=	_____
Independent Claims	____	– 3** =	_____	X _____	=	_____
Multiple Dependent				_____	=	_____

**Or number previously paid, if greater; For Reissues, see below.

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	86	2201	43	Independent claims in excess of 3
1203	290	2203	145	Multiple dependent claim, if not paid
1204	86	2204	43	**Reissue independent claims over original patent
1205	18	2205	9	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) $_____

Based on Form PTO/SB/17 (08-03) as modified by BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP on 09/30/03.

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for ex parte reexamination	
1813	8,800	1813	8,800	Request for inter parties reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	475	Extension for reply within third month	
1254	1,480	2254	740	Extension for reply within fourth month	
1255	2,010	2255	1,005	Extension for reply within fifth month	
1401	330	2401	165	Notice of Appeal	
1402	330	2402	165	Filing a brief in support of an appeal	$330.00
1403	290	2403	145	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive – unavoidable	
1453	1,330	2453	665	Petition to revive - unintentional	
1501	1,330	2501	665	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	2503	320	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	2809	385	For filing a submission after final rejection (see 37 CFR 1.129(a))	
1814	110	2814	55	Statutory Disclaimer	
1810	770	2810	385	For each additional invention to be examined (see 37 CFR 1.129(b))	
1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	
1504	300	1504	300	Publication fee for early, voluntary, or normal pub.	
1505	300	1505	300	Publication fee for republication	
1803	130	1803	130	Request for voluntary publication or republication	
1808	130	1808	130	Processing fee under 37 CFR 1.17(i) (except provisionals)	
1454	1,330	1454	1,330	Acceptance of unintentionally delayed claim for priority	
Other fee (specify)					
Other fee (specify)					

SUBTOTAL (3) $ 330.00

*Reduced by Basic Filing Fee Paid

SUBMITTED BY:

Typed or Printed Name: Daniel E. Ovanezian

Signature: _____ Date: 8/4/04

Reg. Number: 41,236 Telephone Number: (408) 720-8300

Send to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

FIRST CLASS CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to Mail Stop Appeal Brief - Patents, Commissioner for Patents, PO Box 1450, Alexandria, Virginia 22313-1450.

8/4/04
Date of Deposit

JUANITA BRISCOE
Name of Person Mailing Correspondence

Signature

8/4/04
Date

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:	)	Examiner: Song, Jasmine
William R. Stafford	)	Art Unit: 2188
Serial No.: 09/927,252	)	
Filed: August 10, 2001	)	
For: MULTIPLE USER INTERFACES FOR AN INTEGRATED FLASH DEVICE	)	

APPEAL BRIEF
IN SUPPORT OF APPELLANT'S APPEAL
TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

Mail Stop Appeal Brief - Patents
Commissioner for Patents
PO Box 1450
Alexandria, Virginia 22313-1450

Dear Sir:

Appellant hereby submits this Brief in triplicate in support of an appeal from a final decision by the Examiner, mailed on May 5, 2004, in the above-captioned case. Appellant respectfully requests consideration of this appeal by the Board of Patent Appeals and Interferences for allowance of the above-captioned patent application.

Table Of Contents

I. REAL PARTY IN INTEREST

The real party in interest is Intel Corporation, of Santa Clara, California.

II. RELATED APPEALS AND INTERFERENCES

To the best of Appellant's knowledge, there are no appeals or interferences related to the present appeal that will directly affect, be directly affected by, or have a bearing on the Board's decision.

III. STATUS OF CLAIMS

For the purposes of this appeal, claims 19-24 and 26-38 stand rejected. A copy of all claims pending on appeal is attached as Appendix A.

IV. STATUS OF AMENDMENTS

There are currently no pending amendments to claims 19-24 and 26-38.

V. SUMMARY OF THE INVENTION

The present invention concerns a memory device, a component board having the memory device, and a computer system having the memory device.

In one embodiment of the present invention, the memory device includes memory storage and three different interfaces to operate the memory storage in at least one of three different modes. The memory storage and the three different interfaces reside in a common die. (Specification, page 7, lines 1-13 and lines 16-18; page 10 lines 8-11; Figure 2).

In another particular embodiment of the present invention, the memory device is a flash memory. (Specification, page 6, lines 17-19). The flash memory device has a plurality of different interfaces to operate the memory device in a plurality of different modes with one of the plurality of interfaces being a standard flash memory interface. (Specification, page 7, lines 6-13 and 19-21; page 8 lines 7-9; page 10, line 18).

VI. ISSUES

A. Whether claims 19-21, 23-24, 26-29 and 32-35 are unpatentable under 35 U.S.C. § 103(a) as being obvious over U.S. Patent No. 5,815,427 of Cloud et al. ("Cloud") in view of U.S. Patent No. 6,021,469 of Tremblay ("Tremblay").

B. Whether claims 22, 30-31 and 36-37 are unpatentable under 35 U.S.C. § 103(a) in view of Cloud.

C. Whether claim 38 is unpatentable under 35 U.S.C. § 103(a) as being obvious over Cloud.

VII. GROUPING OF CLAIMS

With regard to the ground of rejection stated in issue A, claims 19-21, 23-24, 26-29 and 32-35 stand or fall together.

With regard to the ground of rejection stated in issue B, claims 22, 30-31 and 36-37 stand or fall together. The ground of rejection stated in issue B is different than the ground of rejection stated in issue A and, therefore, claims 22, 30-31 and 36-37 stand or fall separate from claims 19-21, 23-24, 26-29 and 32-35.

With regard to the ground of rejection stated in issue C, claim 38 stands or falls alone. Claim 38 stands or falls separate from either claims 19-21, 23-24, 26-29 and 32-35 or claims 22, 30-31 and 36-37.

VIII. ARGUMENTS

A. Claims 19-21, 23-24, 26-29 and 32-35 are patentable under 35 U.S.C. § 103(a) over Cloud in view of Tremblay.

1. Overview of Cited References and Rejection.

Claims 19-21, 23-24, 26-29 and 32-35 are patentable under 35 U.S.C. § 103(a) over Cloud in view of Tremblay because there is no motivation to modify the cited references in the manner purported by the Examiner. Claims 19, 26 and 32 are independent claims. Claims 20-21 and 23-24 are dependent from base claim 19. Claims 27-29 are dependent from base claim 26. Claims 33-35 are dependent from base claim 32. Each of independent claims 19, 26 and 32 include the limitation of a memory device comprising "memory storage and three different interfaces to operate the memory storage in at least one of three different modes, wherein the memory storage and the three different interfaces reside in a common die."

Cloud teaches a modular circuit that includes a memory module 12 that is formed on a first die, an interface module 14 formed on a second die that has interface circuitry, and a peripheral module 18 such as a microprocessor formed on a third die. The interface module 14 includes interface circuitry, such as conventional input/output (I/O) buffers, that provide an interface between the read/write circuitry of memory module 12 and an external data bus. (Cloud, col. 2, lines 50-53). After assembly of each of the different die modules, the packed modules are mounted to an interconnection module board 16

using a conventional technique such as epoxy bonding. (Cloud, Summary of the Invention, col. 2, lines 1-16; col. 1, line 44 to col. 2, line 4; Figure 1). Cloud teaches that advantages provided by the modularity (i.e., components formed on different package die) of its purported invention are the ability to customize circuits with fewer changes to the processing sequence and with greater speed and cost effectiveness, and the ability to form circuits from partially defective modules. (Cloud, Summary of the Invention, col. 2, lines 1-16).

Tremblay teaches a hardware processor 100 having an I/O controller 111 that interfaces with an instruction cache unit 120 and a DRAM controller 112 that interfaces with a data cache unit 160. The I/O controller 111 and DRAM controller 112 are implemented in a memory interface unit 110 that interfaces with an external memory. As such, there is only a single interface (via memory interface unit 110) with the external memory.

The instruction cache unit of Trembly includes an instruction cache controller 121 that interfaces with instruction cache 125. Data cache unit 160 includes a data cache controller 161 that interfaces with data cache 165. (Tremblay, figure 1, col. 11, lines 23-35 and col. 17, lines 44-45). One of the objects of the teachings in Tremblay is to reduce the expense associated with memory storage on hardware processor 100. (Tremblay, col. 6, lines 3-4 and lines 20-27). In particular, Tremblay advocates the advantage that additional memory storage typically required by a software interpreter is eliminated from the hardware processor 100 described therein by its purported invention. (Trembly, col. 6, lines 3-7).

In rejecting claims 19-21, 23-24, 26-29 and 32-35 of the present application, the Examiner improperly reasoned that:

> It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the teachings of Tremblay in the memory system of Cloud and have the memory storage and the three different interfaces reside in a common die **for the advantage of much better performance characteristics** (col.5, lines 40-42 and col.6, lines 3-5) and not necessarily to arbitrate to use the memory bus since the memory storage and the three different interfaces as hardware processor is the only master (col. 11, lines 27-28 and 39-41).

(Office Action, 3/24/04, page 4)(emphasis added).

2. The Examiner has failed to provide a motivation to combine the cited references in the purported manner.

Despite the Examiner's assertions, Appellant respectfully submits that the Examiner has failed to point out any motivation for the combination of these cited references. Here, the Examiner merely provides a general assertion that the cited references may be combined "for the advantage of much better performance characteristics" without providing an explanation as to the specific understanding or principle within the knowledge of the skilled artisan that would have provided a motivation to combine the teachings of Trembly with that of Cloud. Such a vague and broad generalization cannot serve as a basis for a motivation to combine references. It is submitted that the mere fact that references can be combined or modified is not sufficient to establish prima facia obviousness unless the prior art also suggest the desirability of the combination. *In re Mills*, 916 F.2d 680 (Fed. Cir. 1990); MPEP 2143.01. Furthermore, even if Appellant's claimed invention might be considered a technologically simple concept, the Examiner is still required to provide a specific understanding or principle within the knowledge of the skilled artisan that would have provided the motivation to modify the reference the manner purported by the Examiner. *In re Kotzab*, 217 F.3d 1365, 1371 (Fed. Cir. 2000); MPEP 2143.01.

Since the Examiner has failed to provide the specific understanding or principle within the knowledge of the skilled artisan that would have provided a motivation to combine the teachings of Trembly with that of Cloud, the Examiner has failed to meet the burden to show a motivation for the purported combination and, therefore, has not established a prima facia case of obviousness.

3. One of ordinary skill in the art would not be motivated to combine the teachings of Trembly with that of Cloud.

It is also submitted that the teachings of Tremblay cannot be combined with Cloud for any one or more of the following reasons: (1) a modification of the modular architecture of Cloud with the teachings of Trembly would change the principle of operation of Cloud, (2) Cloud teaches away from integration of component functions, and (3) Tremblay teaches away from using on-die memory storage.

First, modifying Cloud to put the memory storage and the different interfaces on a common die would require substantial reconstruction and redesign of the elements shown in Cloud as well a change in the basic principle under which the modular architecture of Cloud was designed to operate. Cloud teaches a modular circuit that includes a memory module 12 that is formed on a first die, an interface module 14 formed on a second die that has interface circuitry, and a peripheral module 18, such as a microprocessor, formed on a third die. After assembly of each of the different die modules, the packed modules are mounted to an interconnection module board 16 using a conventional technique such as epoxy bonding. (Cloud, Summary of the Invention, col. 2, lines 1-16; col. 1, line 44 to col. 2, line 4; Figure 1). As such, the principle of operation of Cloud is a modular architecture. The Examiner's proposed modification of Cloud to put its memory module

12 and its interface module 14 on a common die would impermissibly change the modular architecture of Cloud and, therefore, does not provide a motivation for modifying Cloud with the teachings of Trembly in the manner purported by the Examiner. MPEP § 2143.01. *In re Ratti*, 270 F.2d. 810 (CCPA 1959).

Second, Cloud teaches away from integration of component functions by stating that custom integrated circuits may be difficult and costly to produce. (Cloud, col. 1, lines 56-58). One of the advantages stated by Cloud of the modularity of its invention is the ability to form circuits from partially defective modules. (Cloud, col. 2, lines 15-16). This further evidences that one of ordinary skill in the art, confronted with the same problems as the inventors of Cloud, and with no knowledge of the Appellant's invention, would not combine elements from Tremblay with Cloud in the manner purported by the Examiner to put memory storage and three different interfaces on a common die. See, *In re Rouffet*, 149 F.3d 1350 (Fed. Cir. 1998). Furthermore, the proposed modification to Cloud would render Cloud unsatisfactory for its intended purposes of providing modularity and reducing production costs. MPEP § 2143.01. See, *In re Gordon*, 733 F.2d 900 (Fed. Cir. 1984).

Third, one of the objects of the teachings in Tremblay is to reduce the expense associated with memory storage on a hardware processor. (Tremblay, col. 6, lines 3-4 and lines 20-27). In particular, Tremblay advocates the advantage that additional memory storage typically required by a software interpreter is eliminated from the hardware processor 100 described therein by its purported invention. Therefore, one of ordinary skill in the art, *facing the problems confronting the inventors* of Cloud, would not only be unmotivated to look to the teachings of Trembly but would be further encouraged to maintain the design approach in Cloud of not using on-die memory storage

in its microprocessor die 18 or interface die 14. See, *In re Rouffet*. Furthermore, the proposed modification would also render Tremblay unsatisfactory for its intended purposes of eliminating on-die memory storage and reducing production costs. MPEP § 2143.01. *In re Gordon*.

a. These Arguments were not sufficiently addressed by the Examiner.

The first and second of these arguments have been presented to the Examiner three times already in Appellant's response to the Office Actions dated 3/24/04, 11/5/03, and 6/4/03 (submitted with the RCE filed on 8/27/03). The third argument was presented in Appellant's response to the Office Action dated 6/4/03. However, the Examiner has never addressed these arguments, despite Appellant's repeated requests for consideration. Rather, the Examiner continues to simply recite the same rejection without further explanation or application to 1) the modular architecture of Cloud, 2) the teaching away by Cloud from integration of component functions, or 3) the teaching away by Tremblay from using on-die memory storage. The Advisory Action dated 5/5/2004 is exemplary of the Examiner's persistent recitation of the unsupported rejection. In particular, the Advisor Action states:

> Response to applicant's argument "the teachings of Trembly cannot be combined with Cloud", the Examiner notices that this argument has been addressed in previous final rejection dated on 03/24/2004 (#9 of the final rejection. (Advisory Action, 5/5/04, page 2) (sic, all).

However, the Examiner never addressed these arguments in section #9 of the Office Action dated 3/24/04 or any other Office Action. Instead, the Examiner restated the unsupported rejection based on "the advantages as noted above," referring to the citation quoted in the text of this argument.

In light of the above, Appellant submits that the Examiner has failed to meet the burden to show a motivation for the purported combination by not providing a specific understanding or principle within the knowledge of the skilled artisan that would have provided a motivation to combine the teachings of the cited references, and that there is not motivation to combine the cited references in the manner purported by the Examiner.

In contrast, independent claims 19, 26 and 32 and the respective dependent claims 20-24, 27-31 and 33-37, recite what is **contrary to the understandings and expectations** of Cloud and Trembly and, therefore, are patentable over the cited references. MPEP 2144.04. *Schenck v. Norton Corp.*, 713 F.2d 782 (Fed. Cir. 1983).

4. The combination of cited references lacks the limitation of "three different interfaces to operate the memory storage in at least one of three different modes" in claims 19-21, 23-24, 26-29 and 32-35.

Claims 19-21, 23-24, 26-29 and 32-35 are patentable under 35 U.S.C. § 103(a) over Cloud in view of Tremblay because the combination of cited references lacks at least one limitation appearing in each of claims 19-21, 23-24, 26-29 and 32-35. The Examiner rejected claims 19-21, 23-24, 26-29, and 32-35 under 35 U.S.C. § 103(a) as being unpatentable over Cloud in view of Tremblay. The Examiner mistakenly reasoned that:

> [Cloud teaches] three different interfaces (Fig.1, element 14 includes three different interfaces which are shown in the Fig.5 and 6) such as the **programming interface** (Fig.5, col.5, lines 45-58), the **test interface** (Fig.6, element 77, col.6, lines 44-47) and operation interface (Fig.6, element 74 and 76, col.6, lines 36-44) to operate the memory storage (Fig.1, element 10) in at least one of three different modes (Fig.5 and 6, col.5, lines 45-48 and col.6, lines 36-47), the **test interface to test the memory device** (Fig.6, element 77, col.6, lines 44-47). [sic, ", and"] the **programming interface to program the memory storage** (Fig.5, col.5, lines 45-58).

(Office Action, 3/24/04, page 3)(emphasis added).[1]

The Examiner attempted to clarify the stated rejection in the Advisory Action dated 5/5/04 by stating:

> Response to the applicant's arguments "The programming of Module 14 and the BIS Circuitry of Module 14 of Cloud are not programming and test interfaces, the Examiner notices that interface can be software that enables a program to work with the user (Microsoft press Computer dictionary, third edition), for example, the programming of the I/O select circuit 55 which considered as programming interface, also, interface can be a card, plug, or other device that connects pieces of hardware with the computer so that information can be moved from place to place (Microsoft Press Computer Dictior, third edition), for example, BIST circuit 77 which considered as test interface.

(Advisory Action, 5/5/04, page 2) (sic, all)

Appellant respectfully submits that the Examiner's characterization of the purported "programming interface" and "test interface" of Cloud is incorrect. The Office Action cites to col. 5, lines 45-48 of Cloud and mischaracterizes the disclosure therein as a "programming interface." The cited passage of Cloud refers to the programming of the I/O select circuit 55 in conventional manners (e.g., laser fuses, antifuses, etc.) to couple an appropriate one of the I/O circuits to the output bus 56. Whether the programming of I/O select circuit 55 is done in using hardware (as taught by Cloud) or software (as purported by the Examiner), such is not a "programming interface" but, rather, the programming of the select circuit to be configured to provide a particular interface to memory module 12.

[1] The Examiner employed identical language from a previous Office Action (Office Action, 11/5/03, page 3) and employed similar language in three earlier Office Actions (Office Action, 6/4/03, page 3, under 35 U.S.C. § 103(a); Office Action, 12/16/02, page 3, under 35 U.S.C. § 102(e); Office Action, 5/17/02, page 3, under 35 U.S.C. § 102(e)).

With respect to the Examiner's assertion that Cloud discloses a test interface, the Office Action mischaracterizes the built-in-self-test (BIST) circuit 77 of Figure 6 as a "test interface" and cites to col. 6, lines 44-47 of Cloud in support thereof. It is respectfully submitted that the cited passage of Cloud refers to a circuit for testing the interface circuitry on module 14. As can be seen by Figure 6 of Cloud, the BIST circuit 77 is coupled to the input buffers 74 and output drivers 76 in order to test these buffers and drivers. As such, the BIST 77 is not an interface itself, test or otherwise, but rather a built-in-self-test circuit to test the interface circuitry (e.g., the input buffers 74 and output drivers 76 form an interface between the module 12 and the DATA bus) on the module 14.

As such, Cloud does not teach three different interfaces as purported by the Examiner. Rather, Cloud teaches only a single interface: interface module that provides an interface between the read/write circuitry of memory module 12 and an external data bus. (Cloud, col. 2, lines 50-53). Furthermore, Trembly teaches only a single interface with external memory: memory interface unit 110.

In contrast, independent claims 19, 26 and 32 and the respective dependent claims 20-24, 27-31 and 33-37, include the limitation of "three different interfaces, wherein the memory storage and the three different interfaces reside in a common die." Cloud and Trembly, either alone or in combination, do not teach or suggest "memory storage and three different interfaces to operate the memory storage in at least one of three different modes, wherein the memory storage and the three different interfaces reside in a common die." Therefore, claims 19-21, 23-24, 26-29 and 32-35 are patentable over the combination of cited references.

B. Claims 22, 30-31 and 36-37 are patentable under 35 U.S.C. § 103(a) over Cloud

Claims 22, 30-31 and 36-37 are patentable under 35 U.S.C. § 103(a) over Cloud because Cloud does not disclose, teach or suggest one of the limitations appearing in each of claims 22, 30-31 and 36-37. Claim 22 is dependent from base claim 19. Claims 30-31 are dependent from base claim 26. Claims 36-37 are dependent from base claim 32. Each of independent claims 19, 26 and 32 include the limitation of a memory device comprising "memory storage and three different interfaces to operate the memory storage in at least one of three different modes, wherein the memory storage and the three different interfaces reside in a common die."

In rejecting claims 22, 30-31 and 36-37, the Examiner incorrectly reasoned:

> Regarding claims 22, 20-31 and 36-38, Cloud et al. teach the limitations in the claims above.

(Office Action, 3/24/04, page 6)

However, earlier in the same office action, the Examiner admitted that Cloud does not teach memory storage and three different interfaces residing in a common die. Specifically, the Examiner stated:

> Cloud does not teach that the memory storage and the three different interfaces reside in a common die.

(Office Action, 3/24/04, page 3)

In contrast to Cloud, each of claims 22, 30-31 and 36-37 include the limitation of "wherein the memory storage and the three different interfaces reside in a common die." Therefore, claims 22, 30-31 and 36-37 are patentable over Cloud because Cloud does not teach the above noted claims limitation as agreed to by the Examiner.

C. Claim 38 is patentable under 35 U.S.C. § 103(a) over Cloud.

Claim 38 is patentable under 35 U.S.C. § 103(a) over Cloud because the cited reference lacks at least one limitation of the claim 38 and there is no motivation to modify Cloud in the manner purported by the Examiner to arrive at Appellant's claim 38. Claim 38 recites:

> A memory device, comprising **a plurality of different interfaces** to operate the memory device in a plurality of different modes, **wherein the memory device is a flash memory and wherein one of the plurality of interfaces is a standard flash memory interface**.

(emphasis added).

The Examiner rejected claim 38 under 35 U.S.C. § 103(a) as being unpatentable over Cloud. In regards to claim 38, the Examiner stated:

> Regarding claims 22, 30-31 and 36-38, Cloud et al. teach the limitations in the claims above. Cloud does not teach the memory device is a flash memory and BIOS memory. However, Cloud indicates that the memory device is SDRAM, but it may be another type of memory device (col. 6, lines 3-7). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the memory device as the BIOSs which store on a flash memory chip that can be upgraded via software. This would have motivated one of ordinary skill in the art to use flash memory chip in a PC so that the BIOS could be updated in place instead of being replaced.

(Office Action, 3/24/04, page 6).

It is submitted that claim 38 is patentable over Cloud because (1) there is no motivation to modify the teachings of Cloud to utilize a "flash memory" as recited in claim 38 and/or (2) Cloud does not teach or suggest "a plurality of interfaces" as recited in claim 38.

1. There is no motivation to modify Cloud to use a flash memory.

Appellant submits that it would be impermissible hindsight, based on Appellant's own disclosure, to combine Cloud with purported skill in the art to arrive at Appellant's claim 38. Moreover, a rote invocation of the high level of skill in the art is not sufficient to supply a motivation to combine references. The burden is on the Examiner to show why one would be so motivated as to come up with a combination. Here, the burden, respectfully, has not been met because no reason why one of ordinary skill in the art would be motivated to combine the cited references has been provided by the *Examiner other than the advantage provided by the applicant's own disclosure.*

The Examiner agrees that Cloud does not teach the memory device is a flash memory and BIOS memory. Moreover, the Examiner's purported motivation for its asserted modification of Cloud appears to be culled from the teachings of the present application (e.g., specification pages 1-2). As such, it appears that the teachings of the present application have been used as a blueprint in arriving at the rejection of claim 38. Such is a clear example of hindsight reconstruction and cannot properly be used as grounds for rejecting claim 38. The Office Action must show a motivation within Cloud as to why one of ordinary skill in the art, facing the problem confronting the inventors of Cloud, would be motivated to make such a purported modification of Cloud that creates the case of obviousness. See e.g., *In re Rouffet.*

In response to the Appellant's arguments the Cloud does not teach a flash memory, the Examiner incorrectly reasoned that:

> Cloud clearly indicates that **another** type of memory device can be used (col. 6, lines 3-7), other type of memory device include the flash memory since the flash memory has the advantage of keeping the content of data stored even the power to the memory is off.

(Office Action, 3/24/04, page 8)(emphasis added).

Appellant respectfully submits that the Examiner is impermissibly reading Cloud to teach something broader than what is actually taught or suggest by the Cloud. Cloud teaches that "[i]n one embodiment of the invention, the memory device 10 is a synchronous dynamic random access memory (SDRAM), although in other embodiments, the memory device 10 may be **another** type of memory device." (Cloud, col. 6 lines 3-6) (emphasis added). Although, Cloud discloses that memory device 10 may be "another type of memory device" (col. 6, lines 3-7) other than a SDRAM, a flash memory is not the "another type of memory device" contemplated, implied, or suggested by Cloud. Rather, the "another type of memory device" contemplated by Cloud is another type of **volatile** memory device. Cloud does not disclose, teach or suggest that "**all**" types or "**any**" type of memory device can be used. Rather, Cloud's statement that merely "another" type of memory device can be used, coupled with its explicit teaching of volatile type memory devices limits the scope of Cloud to another volatile type memory devices other than the previously described SRAM embodiment memory device that loses its stored data when power to the memory is removed (e.g., a DRAM). It is respectfully submitted that Cloud cannot be read to disclose, teach or suggests something beyond what is explicitly or implicitly disclosed, taught or suggested by the reference itself.

Moreover, there is no motivation to modify Cloud in the manner purported by the Examiner. As previously stated, one of the problems confronting the inventors of Cloud, and advantages of the teachings of Cloud, is cost effectiveness. (Cloud, col. 2, lines 1-16). The types of memory devices that Cloud discloses are inexpensive volatile memory devices that lose their stored data when power to the memory is removed. In contrast, a

flash memory device is a non-volatile memory device that retains the contents of data stored within it even after power to the memory is removed. Such a technological feature tends to make flash memory more expensive than volatile memory devices such as the SDRAM and DRAM devices taught by Cloud. As such, one of ordinary skill in the art would not be motivated to look to flash memory devices for solutions to the problems facing the inventors of Cloud due the cost prohibition of flash memory devices in achieving a cost effective solution as required by Cloud. As such, it would not be obvious to combine a flash memory with the teachings of Cloud.

In regards to a motivation to modify Cloud to utilize a flash memory, the Examiner incorrectly reasoned that:

> **[T]he motivation of using SDRAM (cost effectiveness) can be different than the motivation of using flash memory (keeping the content of data stored even the power to the memory is off)**, therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the flash memory device instead of SDRAM for the advantage as noted above.

(Office Action, 3/24/04, page 9)(emphasis added).

Appellant respectfully submits that the Examiners' analysis is inapposite because there is no motivation to modify Cloud to use flash memory. It appears that the Examiner is asserting that a motivation to use SDRAMs in Cloud, a priori, provides a motivation to use flash memory. Appellant submits that such reasoning is flawed because a motivation to use one element does not, a priori, provide a motivation to use a different element.

In addition, the proposed modification of Cloud to use flash memory would render Cloud unsatisfactory for its intended purpose of providing cost effective circuits. One of the problems confronting the inventors of Cloud, and purported advantages of the teachings of Cloud, is cost effectiveness. (Cloud, col. 2, lines 1-16). The types of

memory devices that Cloud discloses are inexpensive volatile memory devices that lose their stored data when power to the memory is removed. In contrast, a flash memory device is a non-volatile memory device that retains the contents of data stored within it even after power to the memory is removed. Such a technological feature tends to make flash memory more expensive than volatile memory devices, such as the SDRAM and DRAM devices taught by Cloud. As such, one of ordinary skill in the art would not be motivated to look to flash memory devices for solutions to the problems facing the inventors of Cloud due the cost prohibition of flash memory devices. Cloud requires a cost effective solution and, as such, it would not be obvious to combine a flash memory with the teachings of Cloud.

The Examiner also improperly cited U.S. Patent No. 6,125,423 of Yamada ("Yamada") in the Office Action dated 3/24/04 to provide a motivation to modify Cloud. Claim 38 was not rejected using Yamada and, therefore, Yamada cannot be used in the analysis for the rejection of claim 38. The Examiner continued to assert Yamada in the Advisory Action dated 5/5/04, which states, "In addition, Yamada's reference is only the backup reference which support the rejection of claim 38, therefore, the final rejection can be made and do not need to be withdrawn." (Advisory Action, 5/5/04, page 2) (sic, all). The use of Yamada as a reference at all, even if purported to be only a "backup reference" (a term that has not meaning under the status, regulations, or MPEP), would require the issuance of a new rejection.

Moreover, even if Yamada were used in a rejection, the combination of Yamada with Cloud would still be improper because such combination would render Cloud unsatisfactory for its intended purpose of providing cost effective circuits. Appellants submit that there can be no motivation to combine references where the proposed

combination would render the prior art unsatisfactory for its intended purpose. MPEP § 2143.01. *In re Gordon*, 733 F.2d 200 (Fed. Cir. 1984). The Examiner recognizes and "agrees that cost effectiveness is one of the problems confronting the inventors of Cloud and advantages of the teachings of Cloud." (Office Action, 3/24/04, p. 8). Recognizing this advantage of Cloud, it is error for the Examiner to dismiss this advantage in asserting that Cloud could be modified to destroy such advantage. In this case, the proposed modification (using more expensive flash memory) would render Cloud unsatisfactory for its intended purposes of providing cost effective circuits. Therefore, there is no motivation to make the proposed modification.

The Examiner failed provide any explanation to this argument within the Advisory Action dated 5/5/04, which states, "In response to applicant's arguments that impermissible Broadening of Cloud teaching, the Examiner notices this argument also has been addressed in previous final rejection dated on 03/24/2004 (#10)." (Advisory Action, 5/5/04, page 2) (sic, all).

Given that Cloud fails to teach the use of flash memory and one of ordinary skill in the art would not be motivated to modify Cloud to use a flash memory as discussed above, it is submitted the Examiner has failed to establish a *prima facie* case of obviousness under 35 U.S.C. § 103(a) of claim 38.

In contrast, claim 38 includes the limitation of a "wherein the memory device is a flash memory." Therefore, claim 38 is patentable over Cloud.

2. Cloud lacks the limitation of "a plurality of interfaces" appearing in Claim 38.

Claim 38 is patentable over Cloud because Cloud does not teach or suggest the limitation of "a plurality of interfaces to operate the memory device in a plurality of different modes" as recited in claim 38.

In regards to claim 38, the Examiner stated:

> Regarding claims 22, 30-31 and 36-38, Cloud et al. teach the limitations in the claims above.

(Office Action, 3/24/04, page 6)(emphasis added).

It appears that the Examiner is relying on the analysis given with respect to the other claims as an analysis for the other claim limitations appearing in claim 38. In that respect, the Examiner mistakenly reasoned that:

> [Cloud teaches] three different interfaces (Fig.1, element 14 includes three different interfaces which are shown in the Fig.5 and 6) such as the **programming interface** (Fig.5, col.5, lines 45-58), the **test interface** (Fig.6, element 77, col.6, lines 44-47) and operation interface (Fig.6, element 74 and 76, col.6, lines 36-44) to operate the memory storage (Fig.1, element 10) in at least one of three different modes (Fig.5 and 6, col.5, lines 45-48 and col.6, lines 36-47), the **test interface to test the memory device** (Fig.6, element 77, col.6, lines 44-47). [sic, ", and"] the **programming interface to program the memory storage** (Fig.5, col.5, lines 45-58).

(Office Action, 3/24/04, page 3)(emphasis added).[2]

The Examiner attempted to clarify the stated rejection in the Advisory Action dated 5/5/04 by stating:

> Response to the applicant's arguments "The programming of Module 14 and the BIS Circuitry of Module 14 of Cloud are not programming and test interfaces, the Examiner notices that interface can be software that enables a program to work with the user (Microsoft press Computer dictionary, third edition), for example, the programming of the I/O select

[2] The Examiner employed identical language from a previous Office Action (Office Action, 11/5/03, page 3) and employed similar language in three earlier Office Actions (Office Action, 6/4/03, page 3, under 35 U.S.C. § 103(a); Office Action, 12/16/02, page 3, under 35 U.S.C. § 102(e); Office Action, 5/17/02, page 3, under 35 U.S.C. § 102(e)).

> circuit 55 which considered as programming interface, also, interface can be a card, plug, or other device that connects pieces of hardware with the computer so that information can be moved from place to place (Microsoft Press Computer Dictior, third edition), for example, BIST circuit 77 which considered as test interface.

(Advisory Action, 5/5/04, page 2) (sic, all)

Appellant respectfully submits that the Examiner's characterization of the purported "programming interface" and "test interface" of Cloud is incorrect. The Office Action cites to col. 5, lines 45-48 of Cloud and mischaracterizes the disclosure therein as a "programming interface." The cited passage of Cloud refers to the programming of the I/O select circuit 55 in conventional manners (e.g., laser fuses, antifuses, etc.) to couple an appropriate one of the I/O circuits to the output bus 56. Whether the programming of I/O select circuit 55 is done in using hardware (as taught by Cloud) or software (as purported by the Examiner), such is not a "programming interface" but, rather, the programming of the select circuit to be configured to provide a particular interface to memory module 12.

With respect to the Examiner's assertion that Cloud discloses a test interface, the Office Action mischaracterizes the built-in-self-test (BIST) circuit 77 of Figure 6 as a "test interface" and cites to col. 6, lines 44-47 of Cloud in support thereof. It is respectfully submitted that the cited passage of Cloud refers to a circuit for testing the interface circuitry on module 14. As can be seen by Figure 6 of Cloud, the BIST circuit 77 is coupled to the input buffers 74 and output drivers 76 in order to test these buffers and drivers. As such, the BIST 77 is not an interface itself, test or otherwise, but rather a built-in-self-test circuit to test the interface circuitry (e.g., the input buffers 74 and output drivers 76 form an interface between the module 12 and the DATA bus) on the module 14.

As such, Cloud does not teach three different interfaces as purported by the Examiner. Rather, Cloud teaches only a single interface: interface module that provides an interface between the read/write circuitry of memory module 12 and an external data bus. (Cloud, col. 2, lines 50-53.

In contrast, claim 38 includes the limitation of "a plurality of interfaces to operate the memory device in a plurality of different modes." Therefore, claim 38 is patentable over Cloud.

IX. CONCLUSION

For the foregoing reasons, Appellant respectfully asserts that claims 19-24 and 26-38 overcome the cited references and, therefore, are patentable. Any dependent claim not specifically addressed are deemed allowable in view of its dependency from an independent claim as argued above. For the reasons presented herein, Appellant respectfully requests removal of the present rejections and allowance of the present claims.

Fee For Filing Notice of Appeal

A check in the amount of $330.00 to cover the fee for filing a Notice of Appeal required under 37 C.F.R. 1.17(b) was previously submitted with a prior Notice of Appeal filed on April 13, 2001.

Fee For Filing a Brief In Support of Appeal

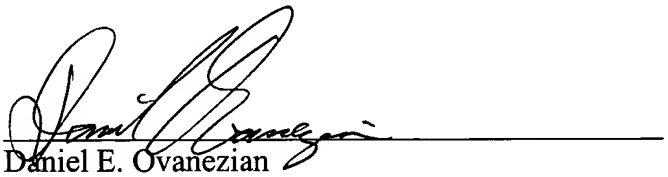
Enclosed is a check in the amount of $330.00 to cover the fee for filing of a brief in support of an appeal required under 37 C.F.R 1.17 (c) and 1.192. This Brief is filed within two months of receipt of the filed Notice of Appeal dated June 24, 2004.

Charge Our Deposit Account

If there are any further charges not accounted for herein, please charge them to our deposit account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 8/4/04 By: 

Daniel E. Ovanezian
Reg. No. 41,236
Attorney for Appellant

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA 90025-1026
408-720-8300

X. APPENDIX A

The claims on appeal read as follows:

19. A memory device, comprising memory storage and three different interfaces to operate the memory storage in at least one of three different modes, wherein the memory storage and the three different interfaces reside in a common die.

20. The memory device of claim 21, further comprising selection circuitry to select among the plurality of different interfaces.

21. The memory device of claim 19, wherein the three different interfaces comprise:

a test interface to test the memory device for defects;

a programming interface to program the memory device with a code; and

an operation interface to operate the memory device in an operation mode.

22. The memory device of claim 21, wherein the memory device is a flash memory and the test interface is a standard flash memory interface.

23. The memory device of claim 21, wherein the operation interface is a proprietary interface.

24. The memory device of claim 20, wherein the selection circuitry comprises:

a plurality of drivers, each of the plurality of drivers coupled between a device pad and a device circuit, each of the plurality of drivers having a control input; and

a multiplexer coupled to the control input of each of the plurality of drivers to select one of the plurality of drivers.

26. A component board, comprising:

a processor; and

a memory device coupled with the processor, the memory device comprising memory storage and three different interfaces to operate the memory storage in at least one of three different modes, where in the memory storage and the three different interfaces reside in a common die.

27. The component board of claim 26, further comprising selection circuitry to select among the three different interfaces.

28. The component board of claim 27, wherein the selection circuitry comprises:

a plurality of drivers, each of the plurality of drivers coupled between a device pad and a device circuit, each of the plurality of drivers having a control input; and

a multiplexer coupled to the control input of each of the plurality of drivers to select one of the plurality of drivers.

29. The component board of claim 26, wherein the three different interfaces comprise:

a test interface to test the memory device for defects;

a programming interface to program the memory device with a code; and

an operation interface to operate the memory device in an operation mode.

30. The component board of claim 29, wherein the memory device is a flash memory, the test interface is a standard flash memory interface, and the operation interface is a proprietary interface.

31. The component board of claim 27, wherein the memory device is a BIOS memory.

32. A computer system, comprising:

a peripheral device; and

a system board coupled to the peripheral device, the system board comprising:

a processor; and

a memory device coupled with the processor, the memory device comprising memory storage and three different interfaces to operate the memory storage in at least one of three different modes, where in the memory storage and the three different interfaces reside in a common die.

33. The computer system of claim 32, further comprising selection circuitry to select among the three different interfaces.

34. The computer system of claim 33, wherein the selection circuitry comprises:

a plurality of drivers, each of the plurality of drivers coupled between a device pad and a device circuit, each of the plurality of drivers having a control input; and

a multiplexer coupled to the control input of each of the plurality of drivers to select one of the plurality of drivers.

35. The computer system of claim 32, wherein the three different interfaces comprise:

a test interface to test the memory device for defects;

a programming interface to program the memory device with a code; and

an operation interface to operate the memory device in an operation mode.

36. The computer system of claim 35, wherein the memory device is a flash memory and the test interface is a standard flash memory interface and the operation interface is a proprietary interface.

37. The computer system of claim 33, wherein the memory device is a BIOS memory.

38. A memory device, comprising a plurality of different interfaces to operate the memory device in a plurality of different modes, wherein the memory device is a flash memory and wherein one of the plurality of interfaces is a standard flash memory interface.